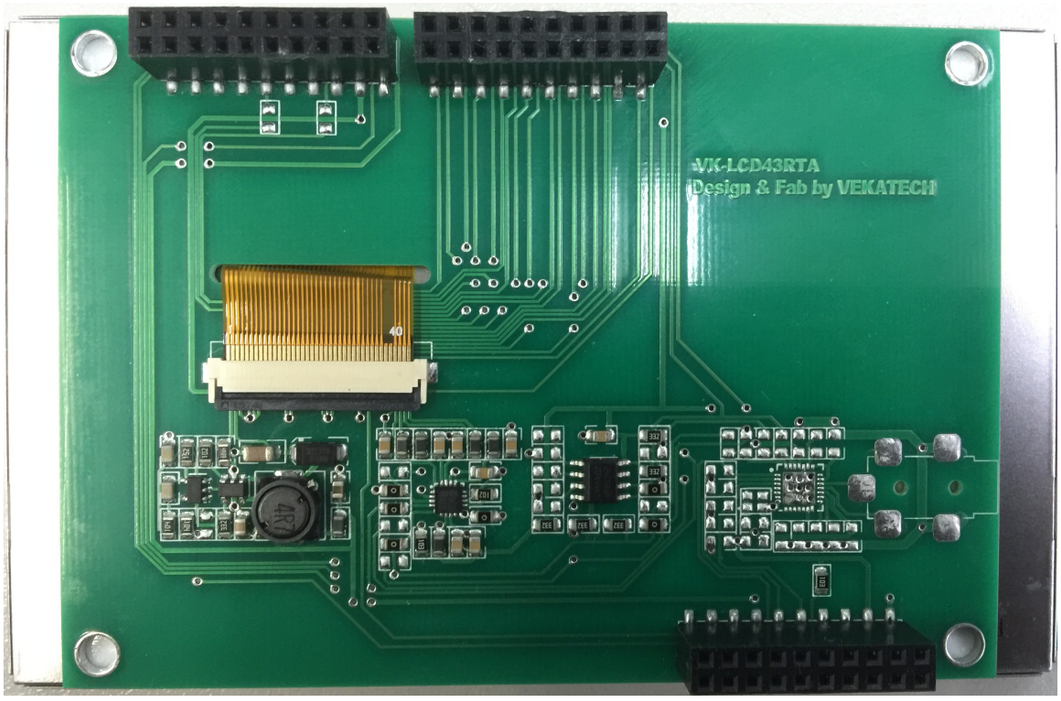
VK-LCD50RTA Display Board

User manual



Rev. 1.0, Oct.15.2015

Revision Changelog	
Rev #	**Description:**
1.0	Initial release
-	-

INTRODUCTION

VK-LCD50RTA is 480 x 272 resistive touchscreen display board. It is designed to be HMI module for VK-RZ/A1H development board.

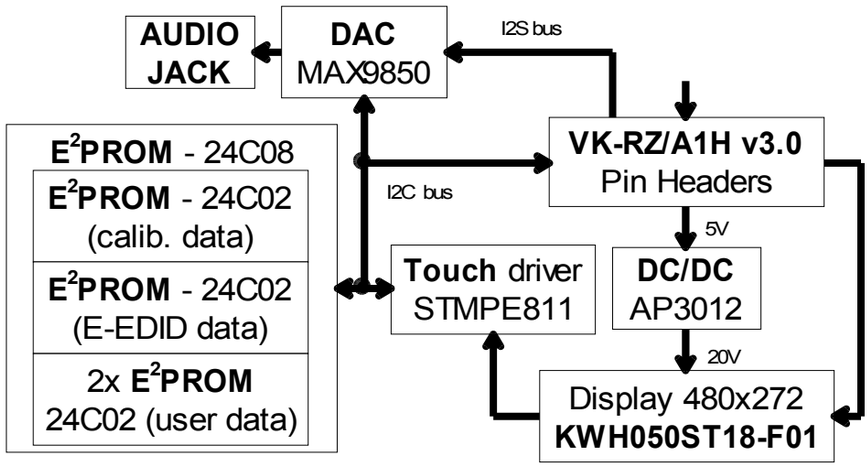
BOARD FEATURES:

- Resistive touch controller: (STMPE811)
- 5 inch resistive display (KWH050ST18-F01)
- E^2PROM (24C08)
- Audio DAC (MAX9850)
- VK-RZ/A1H header connectors (HMI module for VK-RZ/A1H development board)
- Dimensions: (board only 105.0mm x 74.0mm) ,(board with display: 120.7mm x 75.8mm)

ELECTROSTATIC WARNING

VK-LCD50RTA board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

BLOCK DIAGRAM



I^2C ADDRESS SPACE

```
      I2C Slave device address :    0xA8

0x00 – 0x37:      Calibration data        (PROM)      (56  Bytes)
0x38 – 0xFF:      Free user space data    (PROM)      (200 Bytes)

      I2C Slave device address :    0xAA

0x00 – 0x7F:      LCD E-EDID Data         (PROM)      (128 Bytes)
0x80 – 0xFF:      Free user space data    (PROM)      (128 Bytes)
```

```
      I2C Slave device address :    0xAC

0x00 – 0xFF:      Free user space data    (PROM)      (256 Bytes)

      I2C Slave device address :    0xAE

0x00 – 0xFF:      Free user space data    (PROM)      (256 Bytes)
```

⚠ I²C data is accessed with 1 byte addressing !

DATA STRUCTURES

Calibration data has the following meaning:

```
union __CALIB {
  struct __DATA {
    unsigned int len;  // 4 bytes size of calibration structure [bytes]
    unsigned int flag; //4 bytes validation flag (1: constants are valid, 0: they aren't)
    double KX1, KY1, KX2, KY2, KX3, KY3;     // 6 calibration constants [8 bytes each]
  }data;
  unsigned char KX08[sizeof(struct __DATA)]; // 1 byte access to the calibration data
};
```

⚠ ***Screen coordinates are retrieved by the following equation:***

```
Px = (KX1 * raw_x) + (KX2 * raw_y) + KX3 + 0,5;
Py = (KY1 * raw_x) + (KY2 * raw_y) + KY3 + 0,5;
```

where **raw_P(raw_x, raw_y)** is the known raw point from the touch driver and **P(x, y)** is the sought screen point.

*For more information about the calibration procedure please refer to **AN-1021***
(http://www.analog.com/media/en/technical-documentation/application-notes/AN-1021.pdf)

Of course feel free to modify the calibration data in 0x00 – 0x37, by your own desire, using different calibration algorithms.

POWER SUPPLY CIRCUIT:

The consumption of VK-LCD50RTA together with VK-RZ/A1H may vary and the max is 500 mA.

CONFIGURABLE REROUTING

There are features that can be enabled or disabled by manually soldering or desoldering a connections, (mostly 0 Ω resistors). If the user wants to enable given purpose, related designator should be soldered and sometimes some others must be desoldered. Connections with ***** are soldered and these are factory default settings.

Optionals: solder at your own risk, double check & comply with the schematic !			
Designator#	Signal	Purpose	Dependence
Jp1,2	Hsync, Vsync	Allow Hsync, Vsync to go out to J3	
Jp4 *	A0 Data	Set STMPE811 slave address to 0x82	Remove Jp5
Jp5	A0 Data	Set STMPE811 slave address to 0x88	Remove Jp4
Jp6	AP3012 SH	Turn on/off backlight with BL_PWM=0	-
Jp7,9	SDA0, SCL0	Access STMPE811 from I²C0	Remove Jp8,10
Jp8*,10*	SDA3, SCL3	Access STMPE811 from I²C3	Remove Jp7,9
Jp12*,13*,14	A0, A1, A2	Set 24C08 slave address to 0xA8	-
Jp15*,17*	SCL0, SDA0	Access MAX9850 from I²C0	Remove Jp11,16
Jp11.16	SCL3, SDA3	Access MAX9850 from I²C3	Remove Jp15,17
Jp18,20	SCL3, SDA3	Access 24C08 from I²C3	Remove Jp19,21
Jp19*,21*	SCL0, SDA0	Access 24C08 from I²C0	Remove Jp18,20

VK-RZ/A1H V3.0 PIN HEADERS

LCD extension

J9 (RZ/A1H) → J2 (LCD50RTA)			
Pin#	Signal Name	Pin#	Signal Name
1	P1_1/RIIC0SDA	2	P3_0/LCD0_CLK
3	P1_0/RIIC0SCL	4	P3_1/LCD0_TCON0 (DE)
5	P3_9/LCD0_DATA1 (B2)	6	P3_8/LCD0_DATA0 (B1)
7	P3_13/LCD0_DATA5 (G0)	8	P3_12/LCD0_DATA4 (B5)
9	P4_2/LCD0_DATA10 (G5)	10	P3_14/LCD0_DATA6 (G1)
11	P3_11/LCD0_DATA3 (B4)	12	P4_1/LCD0_DATA9 (G4)
13	P4_5/LCD0_DATA13 (R3)	14	P4_4/LCD0_DATA12 (R2)
15	P4_7/LCD0_DATA15 (R5)	16	P4_6/LCD0_DATA14 (R4)
17	P4_0/LCD0_DATA8 (G3)	18	P3_10/LCD0_DATA2 (B3)
19	P3_15/LCD0_DATA7 (G2)	20	P4_3/LCD0_DATA11 (R1)

J10 (RZ/A1H) → J3 (LCD50RTA)			
Pin#	Signal Name	Pin#	Signal Name
1	+5V	2	GND
3	P1_4/RIIC2SCL (n.c. LCD50RTA)	4	+3V3
5	P1_2/IRQ0	6	P1_3/RIIC1SDA (n.c. to LCD50RTA)
7	P1_5/RIIC2SDA (n.c. LCD50RTA)	8	P1_6/RIIC3SCL
9	P3_2/LCD0_TCON1 (Hsync)	10	P1_7/RIIC3SDA
11	P7_8/IRQ1 (n.c. to LCD50RTA)	12	P3_7/LCD0_TCON6 (Vsync)
13	P5_0/TXCLKOUTP (n.c. 50RTA)	14	P5_1/TXCLKOUTM (n.c. to LCD50RTA)
15	P5_2/TXOUT2P(n.c. LCD50RTA)	16	P5_3/TXOUT2M (n.c. to LCD50RTA)
17	P5_4/TXOUT1P(n.c. LCD50RTA)	18	P5_5/TXOUT1M (n.c. to LCD50RTA)
19	P5_6/TXOUT0P(n.c. LCD50RTA)	20	P5_7/TXOUT0M (n.c. to LCD50RTA)

J14 (RZ/A1H) → J4 (LCD50RTA)			
Pin#	Signal Name	Pin#	Signal Name
1	n.c	2	Battery (n.c. to LCD50RTA)
3	n.c	4	n.c
5	P8_10 (n.c. to LCD50RTA)	6	P8_8/TxD3 (n.c. to LCD50RTA)
7	P8_11 (n.c. to LCD50RTA)	8	P8_9/RxD3 (n.c. to LCD50RTA)
9	P8_13/SSIWS4	10	P8_12/SSISCK4
11	P8_15/TIOC2B (BL PWM)	12	P8_14/SSIDATA4
13	P9_1 (n.c. to LCD50RTA)	14	P9_0 (ON/OFF DISPLAY)
15	n.c	16	+1V18 (n.c. to LCD50RTA)
17	RESET (n.c. to LCD50RTA)	18	+3V3
19	GND	20	+5V

SCHEMATICS: