

VK-RZ/A1H Development Board

for Renesas Electronics RZ/A1H ARM Cortex-A9 LSI

ver. 4.0

R7S721000VCBG#YJ0

- 400MHz, 256 BGA, Fanless

10 MByte OnChip RAM

- Can RUN without ext. SDRAM

Up to 128 MByte NOR-Flash

- QSPI, 66MHz, Quad (Burst),8-bit
- Direct fetch is possible

Up to 128 MByte SDRAM

- 66MHz, 16-bit

2 x USB Host/Function

- USB 2.0

Micro SD

- Boot capability

USB Mini-B to UART

- LPC11U35FHI33/501

Ethernet 10/100Base TX

- PHY: LAN8710A-EZK

CAN

- PHY:TJA1040T/VM.118

Atmel CryptoAuthentication:

- ATSHA204A-SSHDA-T

Video In:

- WXGA
- PAL
- NTSC

Video outputs:

- LVDS
- RGB

Exp. Ports:

- RZ/A1 - 97 I/O 3.3V

Debug ports:

- RZ/A1 J-TAG 2x10 pins
- CMSIS DAP SWD interface

DC IN +5V

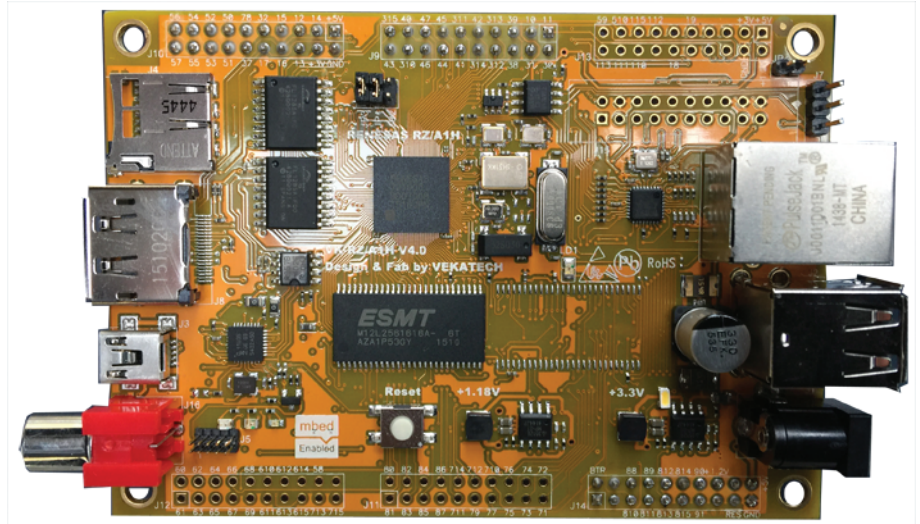
- Consumption +3.3V @ 450mA max

Operating temperature:

- -40 ... +85°

Dimensions:

- ID-2 105 x 74 mm



Board Support Package for:

- u-boot, Linux - GCC
- FreeRTOS - IAR
- CycloneTCP - IAR
- Express Logic Embedded GUI demo - IAR
- IS2S MicroEJ demos - IAR
- .NET Micro Framework - GCC
- MBED enabled

Utilities:

- SD CARD RAM/Flash Loader

Companion boards:

- VK-LCD50RTA - 5" Parallel(65536 colors) TFT LCD display, 480x272, resistive touch(STMPE811), 8kbits i2C memory and Audio DAC(MAX9850)
- VK-LCD70RT - 7" LVDS (65536 colors) TFT LCD display, 1024x600, resistive touch(STMPE811), 8kbits i2C memory

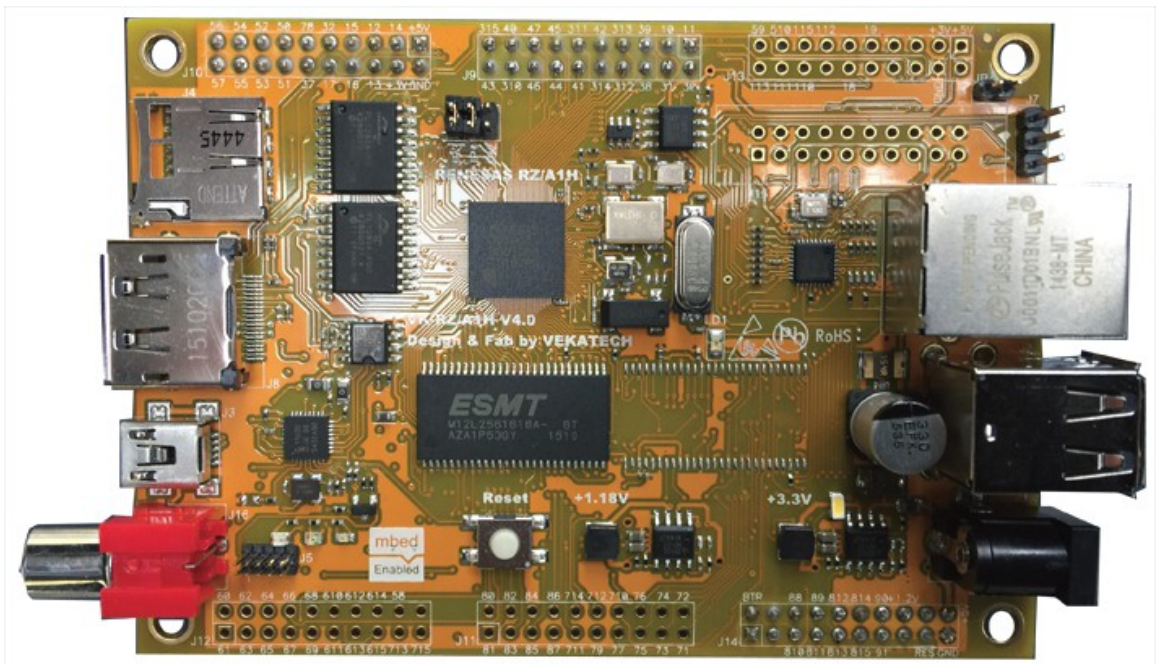
Vekatech Ltd.

59, Sankt Peterburg blvd.
4017 Plovdiv
Bulgaria
Tel.: +359 (0) 32 262362
info@vekatech.com

www.vekatech.com



VK-RZ/A1H Development Board V4.0 User manual



Rev. 4.0, Apr. 1. 2016
Copyright(c) Vekatech Ltd, All right reserved

INTRODUCTION

VK-RZ/A1 is a starter kit which uses MCU R7S721000VCBG from Renesas Electronics. This powerful MCU is actually LSI, single-chip microcontroller that includes an ARM Cortex™-A9 processor along with the integrated peripheral functions required to configure a system. The core includes:

- 32-KB L1 instruction cache
- 32-KB L1 data cache
- 128-KB L2 cache.

Integrated various on-chip peripheral functions and interfaces such as:

- 10-MB large-capacity RAM (128 KB are shared by the data-retention RAM)
- data-retention RAM
- multi-function timer pulse unit 2, OS timer, realtime clock
- motor control PWM timer
- UART, UART with FIFO, I2C, SPI, SPI multi I/O bus controller, CAN, LIN
- serial sound interface, sound generator, CD-ROM decoder
- A/D converter, SCUX
- media local bus, SD host interface, MMC host interface
- NAND flash memory controller
- IEBus™ controller, Renesas SPDIF interface
- Ethernet controller, EthernetAVB
- USB 2.0 host/function
- digital video decoder, video display controller 5
- dynamic range compression, image renderer, image renderer for display
- display out comparison unit
- Renesas graphics processor for OpenVG™
- JPEG codec unit, capture engine unit, pixel format converter
- interrupt controller modules, general I/O ports

The kit supports:

- CAN
- Ethernet
- LVDS Port (optional)
- up to 128 MB SDRAM
- up to 640 MB SPI Flash
- I²C RTC, I²C CryptoAuth (optional)
- Mini SD card connector
- Composite video connector (optional)
- on board debugger
- 2 USB communication channels

All this along with the DC/DC power supply, on board mbed CMSIS-DAP debugger (LPC11U35) and R7S721000VCBG, allow you to build a diversity of powerful applications to be used in a wide range of embedded tasks.

BOARD FEATURES:

- MCU: LPC11U35 - (LPC11U35FHI33/501)
- LSI: RZ/A1H - (R7S721000VCBG)
- USB Mini B device connector (LPC11U35)
- 2xUSB Standard A host connectors (RZ/A1H)
- Micro SD card connector (RZ/A1H)
- Composite video connector (RZ/A1H)
- LVDS Port connector (RZ/A1H)
- CAN connectors (NXP TJA1040) - (RZ/A1H)
- RJ-45 ethernet connector 10/100Mb MAC (PHY SMSC LAN8710A) - (RZ/A1H)
- SDRAM 32 MB (CS2, 64MB per chip select) - (RZ/A1H)
- 4 bit SPI Flash (2x16 Mbits Spansion S25FL128S) - (RZ/A1H)
- I²C RTC with battery holder (ST M41T82) - (RZ/A1H)
- I²C CryptoAuthentication (Atmel ATSHA204) - (RZ/A1H)
- 20 pins Debug/programming connector (JTAG ↔ RZ/A1H)
- 10 pins Debug/programming connector (SWD ↔ LPC11U35)
- Power connector for DC/DC (In: 5V → Out: 3V3 & 1V18)

- FR-4, 2.0 mm, Orange/Blue/Red solder mask, component print
- Dimensions: 105.0mm x 74.0mm

ELECTROSTATIC WARNING

The VK-RZ/A1H - R7S721000VCBG board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

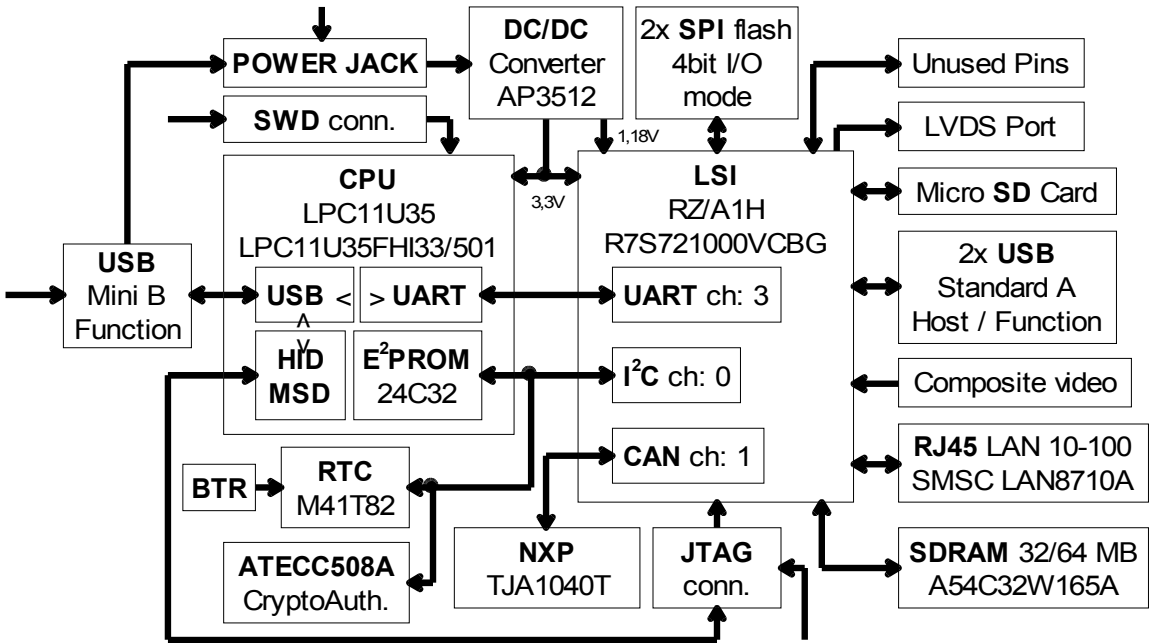
PROCESSOR FEATURES

The VK-RZ/A1H board use MCU R7S721000VCBG from RENESAS ELECTRONICS with these features:

- Power supply voltage: VDD = 3.0 to 3.6 V
- Operating ambient temperature: TA =-40 to +85°C
- Max. CPU clock (I ϕ) = 400 MHz)

For more information please visit www.renesas.eu

BLOCK DIAGRAM



EXTERNAL SDRAM BASE ADDRESSES

SDRAM CS2:	ORIGIN = 0x08000000,	LENGTH = 64MB
SDRAM CS3:	ORIGIN = 0x0C000000,	LENGTH = 64MB
SDRAM CS2 mirror:	ORIGIN = 0x48000000,	LENGTH = 64MB
SDRAM CS3 mirror:	ORIGIN = 0x4C000000,	LENGTH = 64MB

⚠ SDRAM is accessed with 16bit data width

⚠ A14 & A15 are used for bank switching

SCHEMATICS

Please refer to CD for high quality pictures.

POWER SUPPLY CIRCUIT:

VK-RZ/A1H is powered by (5) VDC applied at the power jack.
VK-RZ/A1H could also be powered by USB Mini B connector.
The consumption of VK-RZ/A1H may vary and the maximum is (@3.3V) 450mA.

CLOCK CIRCUITS:

Quartz Generator 13.3333 MHz is connected to **EXTAL**, pin# **AA14**.
Quartz crystal 32.768KHz is connected to **RTC_X1/RTC_X2**, pins# **AA7/Y7**.
Quartz crystal 4.0000MHz is connected to **RTC_X3/RTC_X4**, pins# **V10/V11**.
Quartz crystal 48.0000MHz is connected to **USB_X1/USB_X2**, pins# **AA13/Y13**.
Quartz crystal 27.0000MHz is connected to **VIDEO_X1/VIDEO_X2**, pins# **W21/V20**.
Quartz crystal 22.5792MHz is connected to **AUDIO_X1/AUDIO_X2**, pins# **V21/U20**.
Quartz crystal 25.0000MHz is connected to Ethernet Phy - **SMSC LAN8710A** – (XTAL1/XTAL2, pins# 5/4).
Quartz crystal 12.0000MHz is connected to **LPC11U35** - (XTALIN/XTALOUT, pins# 4/5).
Quartz crystal 32.768KHz is connected to RTC – **M41T82 (XI/XO**, pins# 1/2).

PUSH BUTTONS

Button#	Function	Signal Name	Pin#
SW1	RESET	RESET	U9

JUMPERS CONFIGURATION (Connected Disconnected)

-  **MD_BOOT0** input is constantly tied to '1' (3V3), so only **Boot Mode 3/4/5** are available !
-  **MD_BOOT1** input is tied to **JP1** and **MD_BOOT2** to **JP2**.
-  **MD_CLK** input is constantly tied to '0' (GND), so the LSI is clocked from **EXTAL**.
-  **BSCANP** input is constantly tied to '0' (GND), so the LSI is in normal debug interface mode (i.e. JTAG is connected to **CoreSight debug TAP controller**).

BOOT configuration:

BOOT mode#	JP1,	JP2	Description
3			Boot from SPI multi I/O ch0 : [P9_2 - P9_5]
4			Boot from SD card ch0 : [P4_10 - P4_15]
5			Boot from MMC card ch0 : [P5_10 - P5_15]

Clock settings:

CLK mode#	JP3	Description
MD_CLKS		SSCG circuit OFF
MD_CLKS		SSCG circuit ON

CAN Termination:

CAN mode#	JP4	Description
0		CAN line is terminated
1		CAN line isn't terminated

EXTERNAL CONNECTORS DESCRIPTION

PWR J1			
Pin#	Signal Name	Pin#	Signal Name
1	+5V	2,3	GND

 The power input should be +(5VDC)

SWD 10pin connector

SWD J5			
Pin#	Signal Name	Pin#	Signal Name
1	+3V3	2	MBED_SW D
3	GND	4	MBED_SW C
5	GND	6	-
7	GND	8	-
9	GND	10	MBED_RST

JTAG 20pin connector

JTAG J15			
Pin#	Signal Name	Pin#	Signal Name
1	+3V3	2	+3V3
3	TRST	4	GND
5	TDI/JPO_0	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	-	12	GND
13	TDO/JPO_1	14	GND
15	SRST	16	GND
17	-	18	GND
19	-	20	GND

CAN 3pin connector

CAN J7	
Pin#	Signal Name
1	CAN_L
2	GND
3	CAN_H

CTX1 is connected to P5_10 pin# A7 of R7S721000VCBG.

CRX1 is connected to P5_9 pin# B7 of R7S721000VCBG.

 Termination Jumper JP4.

Ethernet connector RJ45 type: J2

 Transformer and integrated LED S are connected to PHY interface LAN8710A.

 Respective signals from PHY are connected to MII interface of R7S721000VCBG.

USB devices

USB mini B J3			
Pin#	Signal Name	Pin#	Signal Name
1	V_USB1	3	D+
2	D-	5	GND

 Pin#4 ID is disconnected.

V_USB1 Output USB device power.

D- is connected to USB_DM, pin#13 of LPC11U35.

D+ is connected to USB_DP, pin#14 of LPC11U35.

USB standard A J6 (lower)				USB standard A J6 (upper)			
Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name
1	+5V	3	D+	5	+5V	7	D+
2	D-	4	GND	6	D-	8	GND



Both USB are configured as hosts !

lower D- is connected to **DM1**, pin#**AA9** of **R7S721000VCBG**

lower D+ is connected to **DP1**, pin#**Y9** of **R7S721000VCBG**.

upper D- is connected to **DM0**, pin#**AA11** of **R7S721000VCBG**.

upper D+ is connected to **DP0**, pin#**Y11** of **R7S721000VCBG**.

Micro SD card slot:

Micro SD J4			
Pin#	Signal Name	MCU PIN#	MCU PORT
1	DAT2	F18	P4_15/SD_D2_0
2	CD/DAT3	F17	P4_14/SD_D3_0
3	CMD	G20	P4_13/SD_CMD_0
4	VDD	-	-
5	CLK	H21	P4_12/SD_CLK_0
6	GND	-	-
7	DAT0	G18	P4_11/SD_D0_0
8	DAT1	H20	P4_10/SD_D1_0
9	S1	-	-
10	G1	-	-
11	S2	J21	P4_8/SD_CD_0
12	G2	-	-

Composite video

Composite video J16			
Pin#	Signal Name	Pin#	Signal Name
1	VIN1A	2	GND

LVDS port connector: J8

LVDS port J8			
Pin#	Signal Name	MCU PIN#	MCU PORT
1	ML_LANE_0_+	B9	P5_6/TXOUT0P
2	GND	-	-
3	ML_LANE_0_-	A9	P5_7/TXOUT0M
4	ML_LANE_1_+	D10	P5_4/TXOUT1P
5	GND	-	-
6	ML_LANE_1_-	D9	P5_5/TXOUT1M
7	ML_LANE_2_+	B10	P5_2/TXOUT2P
8	GND	-	-
9	ML_LANE_2_-	A10	P5_3/TXOUT2M
10	AUX_CH_+	B11	P5_0/TXCLKOUTP
11	GND	-	-
12	AUX_CH_-	A11	P5_1/TXCLKOUTM
13	-	-	-
14	-	-	-
15	I2C_SCL_3	E13	P1_6/I2C_SCL_3
16	GND	-	-
17	I2C_SDA_3	D13	P1_7/I2C_SDA_3
18	LVDS_HPD	K1	P7_8/IRQ1
19	GND	-	-
20	+3V3	-	-



The signals, that are coming out from the connector, **ARE NOT DISPLAY PORT SIGNALS**, regardless of the fact that the connector is the same as Display port.

CONFIGURABLE REROUTING

There are function and features that can be enabled or disabled by manually soldering or desoldering components, (mostly resistors). Every component, specified with attribute **DNP** is missing by default. If the user wants to enable given Feature, related designator should be soldered and sometimes some other components should be desoldered.

Solder at your own risk, double check & comply with the schematic !			
Designator#	Sheet	Feature	Dependence
R2	Jumper & Pull-Ups	clock the PHY from P5_9	Remove R3 or R179
R6	LAN	Some Oscillator need it	-
R114	LVDS	Lane 0 impedance match	-
R115	LVDS	Lane 1 impedance match	-
R116	LVDS	Lane 2 impedance match	-
R117	LVDS	Lane aux impedance match	-
R126	LVDS	Access LCD EEPROM from I ² C0	Remove R122
R127	LVDS	Access LCD EEPROM from I ² C0	Remove R120
R131	Jumper & Pull-Ups	Drive LD1 from P1_5	Remove R132
R133	Jumper & Pull-Ups	Drive LD1 from P8_10	Remove R132
R145	MCU Control	clock LSI from USB_X1	Remove R152
R147	MCU Control	Set debug mode to boundary scan	Remove R153
R176	mbed-IF	Access RL78 EEPROM from I ² C3	Remove R175
R177	mbed-IF	Access RL78 EEPROM from I ² C3	Remove R174
R194	CAN	Put can transceiver in silent mode	Remove R193
R198	RTC & Crypto	Access RTC & Crypto from I ² C3	Remove R201
R200	RTC & Crypto	Access RTC & Crypto from I ² C3	Remove R199
R210	Memory	Invert SD Card detect signal logic	-
U8	MCU Decoupling	If External Reff. Voltage needed	-

UNUSED PIN HEADERS

LCD extension

J9 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	P1_1/RIIC0SDA	2	P3_0/LCDO_CLK
3	P1_0/RIIC0SCL	4	P3_1/LCDO_TCON0 (DE)
5	P3_9/LCDO_DATA1 (B2)	6	P3_8/LCDO_DATA0 (B1)
7	P3_13/LCDO_DATA5 (G0)	8	P3_12/LCDO_DATA4 (B5)
9	P4_2/LCDO_DATA10 (G5)	10	P3_14/LCDO_DATA6 (G1)
11	P3_11/LCDO_DATA3 (B4)	12	P4_1/LCDO_DATA9 (G4)
13	P4_5/LCDO_DATA13 (R3)	14	P4_4/LCDO_DATA12 (R2)
15	P4_7/LCDO_DATA15 (R5)	16	P4_6/LCDO_DATA14 (R4)
17	P4_0/LCDO_DATA8 (G3)	18	P3_10/LCDO_DATA2 (B3)
19	P3_15/LCDO_DATA7 (G2)	20	P4_3/LCDO_DATA11 (R1)

J10 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	+5V	2	GND
3	P1_4/RIIC2SCL	4	+3V3
5	P1_2/RIIC1SCL	6	P1_3/RIIC1SDA
7	P1_5/RIIC2SDA	8	P1_6/RIIC3SCL
9	P3_2/LCDO_TCON1 (Hsync) On/Off	10	P1_7/RIIC3SDA
11	P7_8/IRQ1	12	P3_7/LCDO_TCON6 (Vsync) (BKL_EN)
13	P5_0/TXCLKOUTP	14	P5_1/TXCLKOUTM
15	P5_2/TXOUT2P	16	P5_3/TXOUT2M
17	P5_4/TXOUT1P	18	P5_5/TXOUT1M
19	P5_6/TXOUT0P	20	P5_7/TXOUT0M

SDRAM extension

J11 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	P8_1/A9	2	P8_0/A8
3	P8_3/A11	4	P8_2/A10
5	P8_5/A13	6	P8_4/A12
7	P8_7/A15	8	P8_6/A14
9	P7_11/A3	10	P7_14/A6
11	P7_9/A1	12	P7_12/A4
13	P7_7/WE1/DQMLU	14	P7_10/A2
15	P7_5/RD/WR	16	P7_6/WE0/DQMLL
17	P7_3/CAS	18	P7_4/CKE
19	P7_1/CS3	20	P7_2/RAS

J12 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	P6_1/D1	2	P6_0/D0
3	P6_3/D3	4	P6_2/D2
5	P6_5/D5	6	P6_4/D4
7	P6_7/D7	8	P6_6/D6
9	P6_9/D9	10	P6_8/D8
11	P6_11/D11	12	P6_10/D10
13	P6_13/D13	14	P6_12/D12
15	P6_15/D15	16	P6_14/D14
17	P7_13/A5	18	P5_8/CS2
19	P7_15/A7	20	n.c

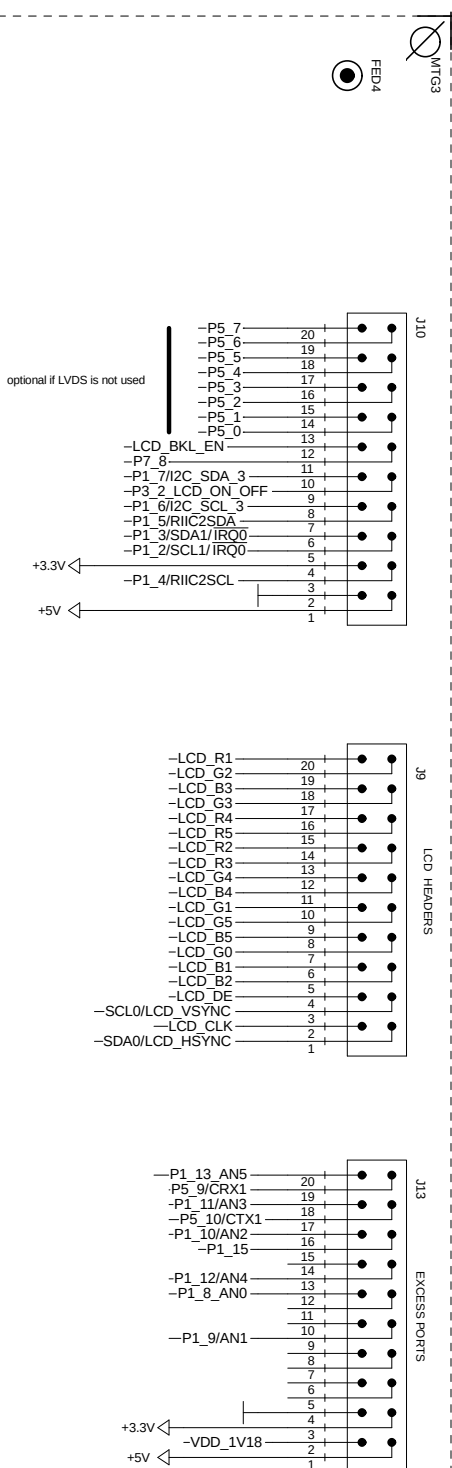
PORT extension

J13 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	+5V	2	+1V18
3	+3V3	4	GND
5	n.c	6	n.c
7	n.c	8	n.c
9	P1_9/AN1	10	n.c
11	n.c	12	P1_8/AN0
13	P1_12/AN4	14	n.c
15	P1_15/AN7	16	P1_10/AN2
17	P5_10/CAN1TX	18	P1_11/AN3
19	P5_9/CAN1RX	20	P1_13/AN5

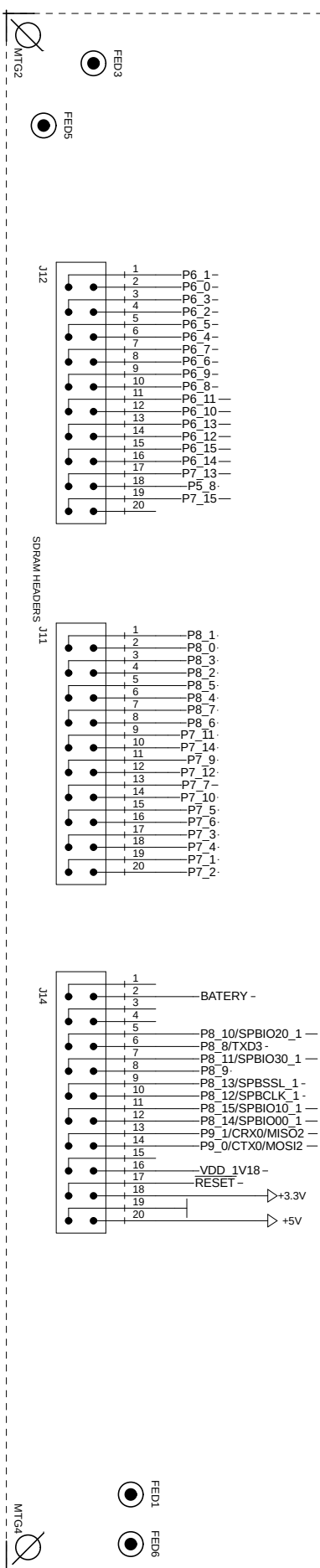
J14 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	n.c	2	Battery
3	n.c	4	n.c
5	P8_10	6	P8_8/TxD3
7	P8_11	8	P8_9/RxD3
9	P8_13	10	P8_12
11	P8_15	12	P8_14
13	P9_1	14	P9_0
15	n.c	16	+1V18
17	RESET	18	+3V3
19	GND	20	+5V

AVAILABLE DEMO SOFTWARE:

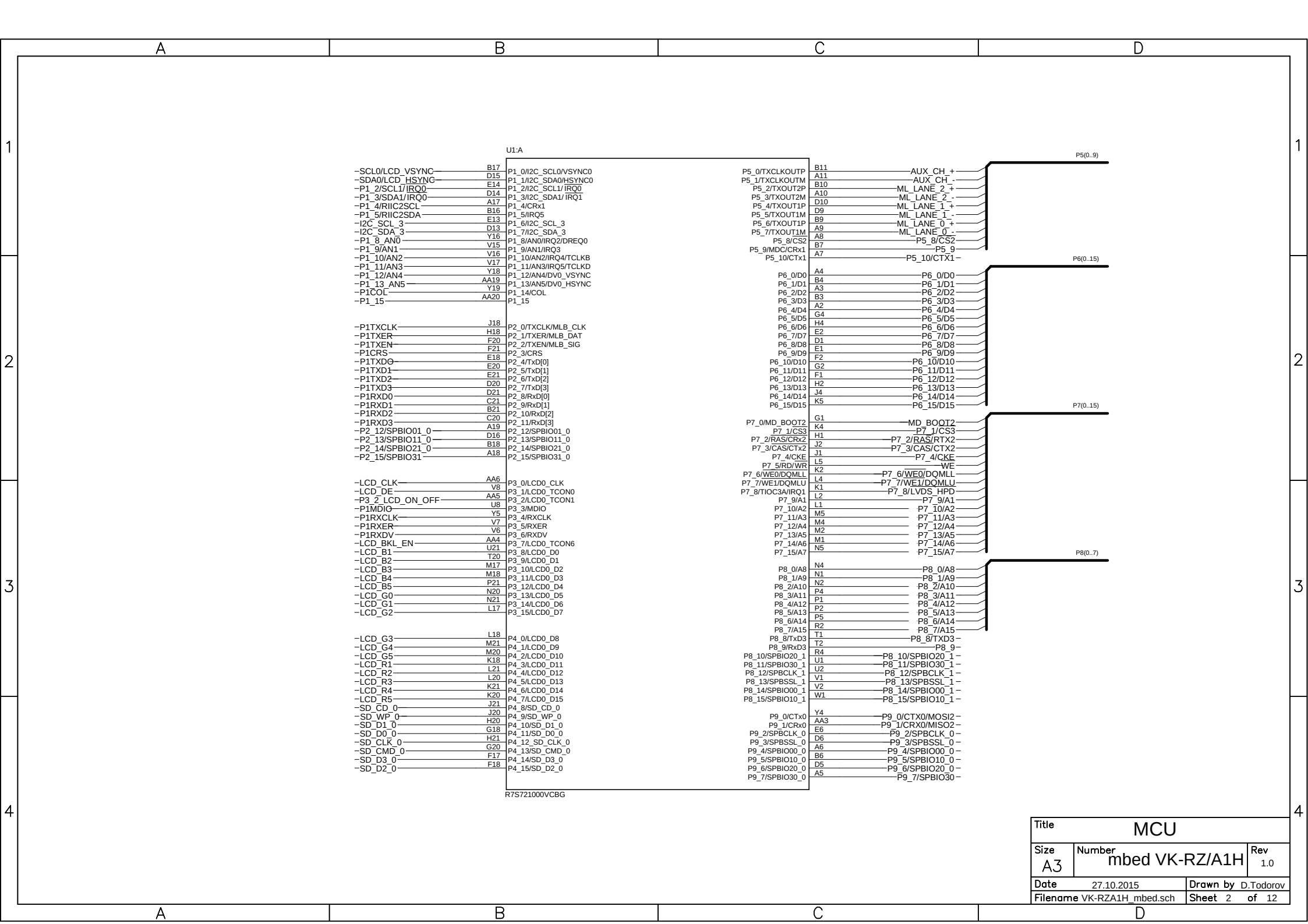
[Demos](#)



mbed VK-RZ/A1H V1.0
Design & Fab by VEKATECH



Title		User I/O	
Size	Number	Rev	
A3	mbed VK-RZ/A1H	1.0	
Date	27.10.2015	Drawn by D.Todorov	
Filename VK-RZ/A1H_mbed.sch		Sheet 1	of 12



1

1

2

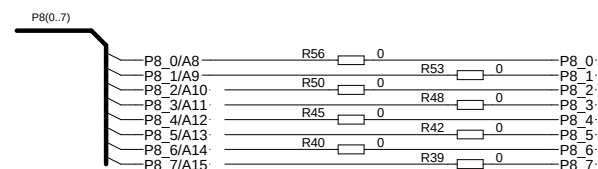
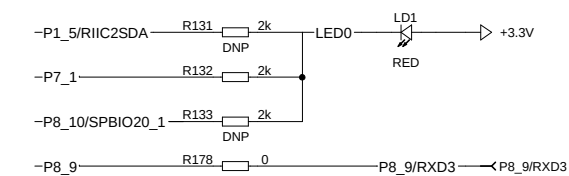
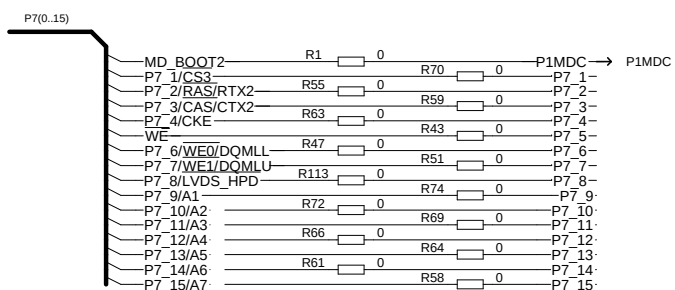
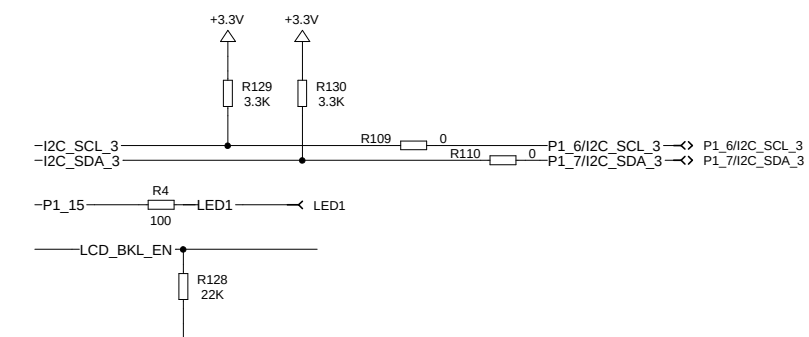
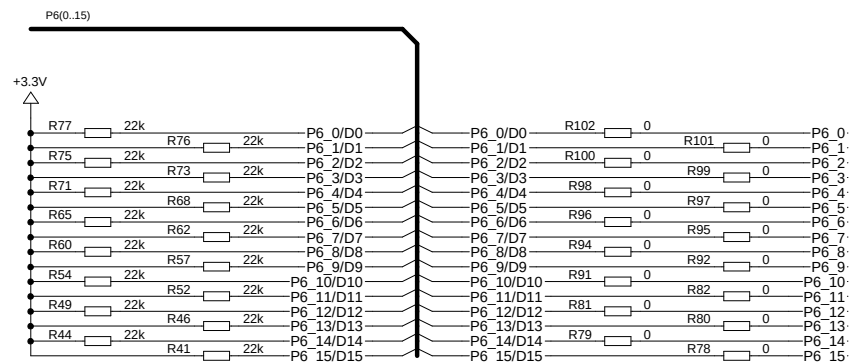
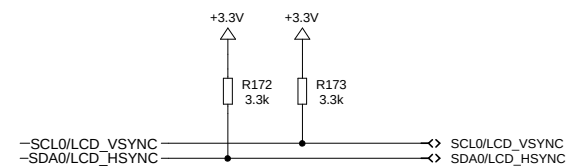
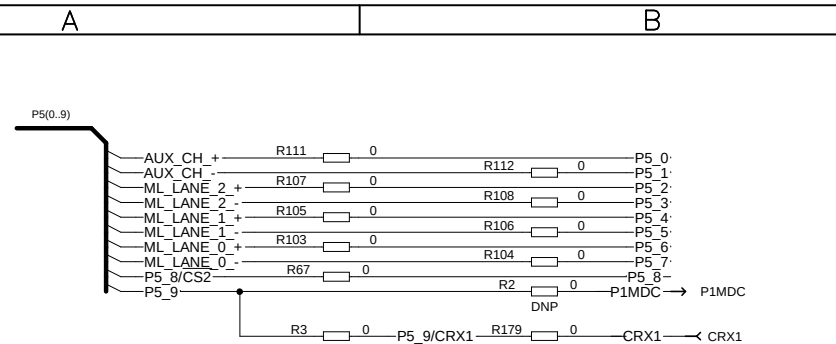
2

3

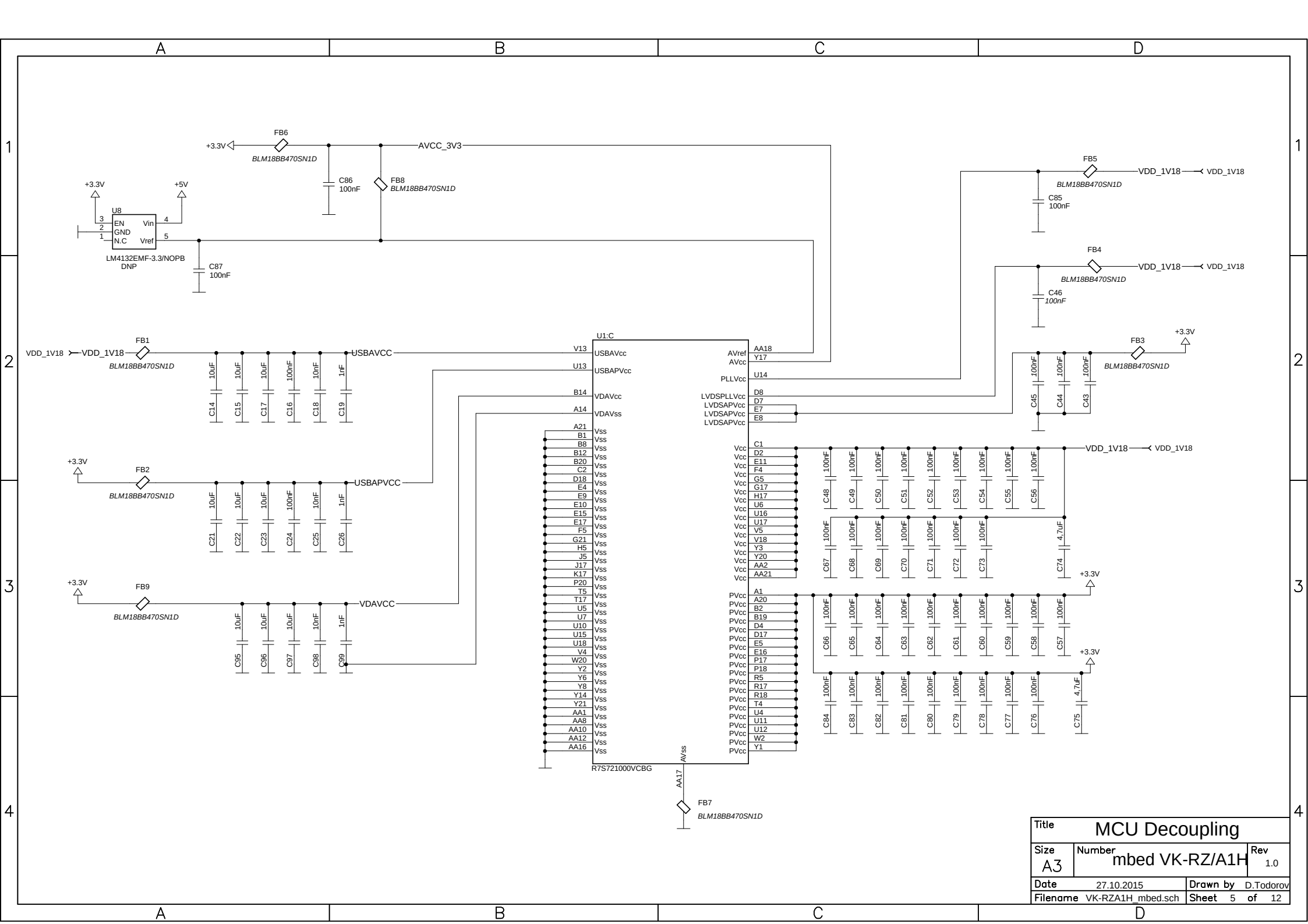
3

4

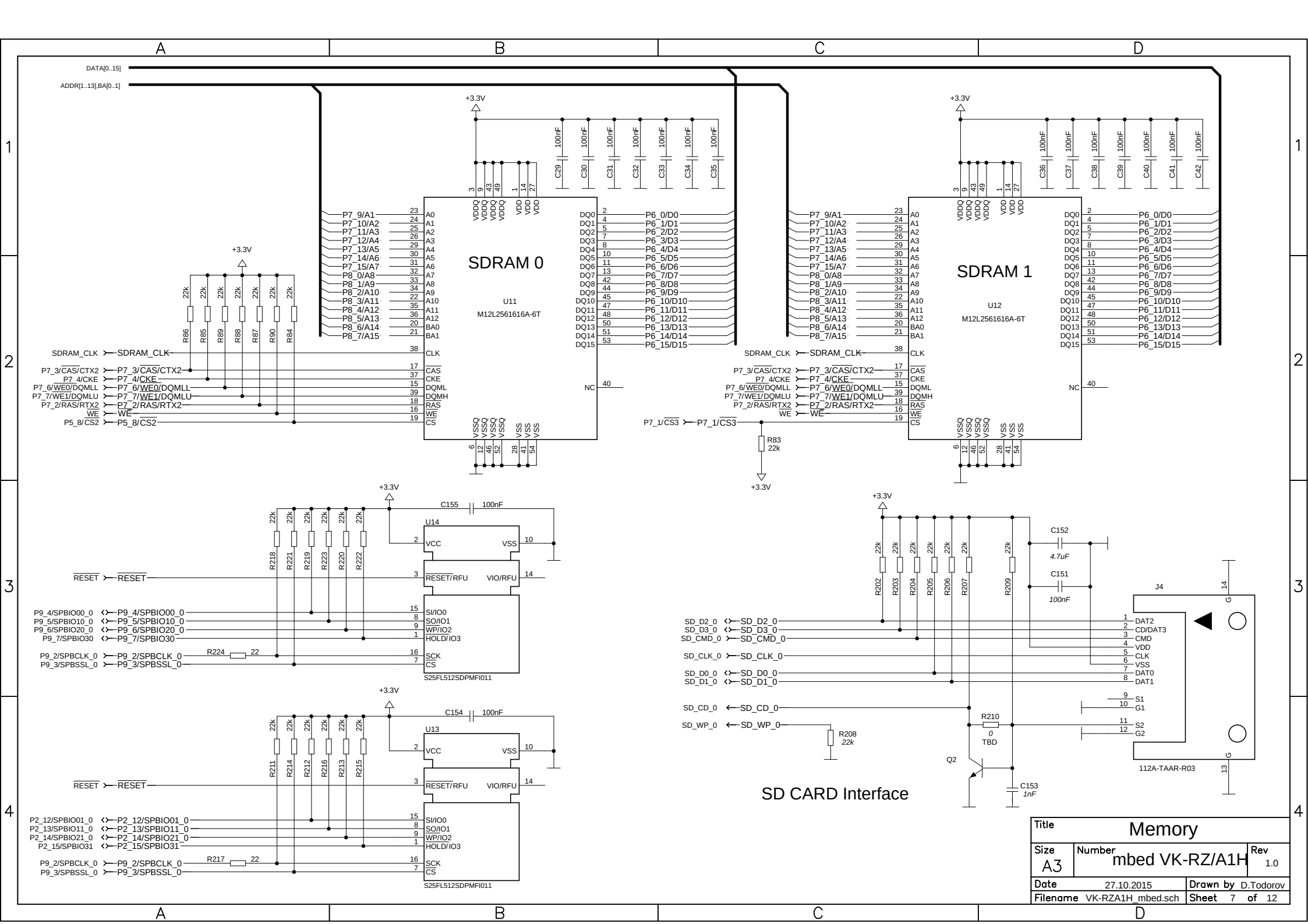
4



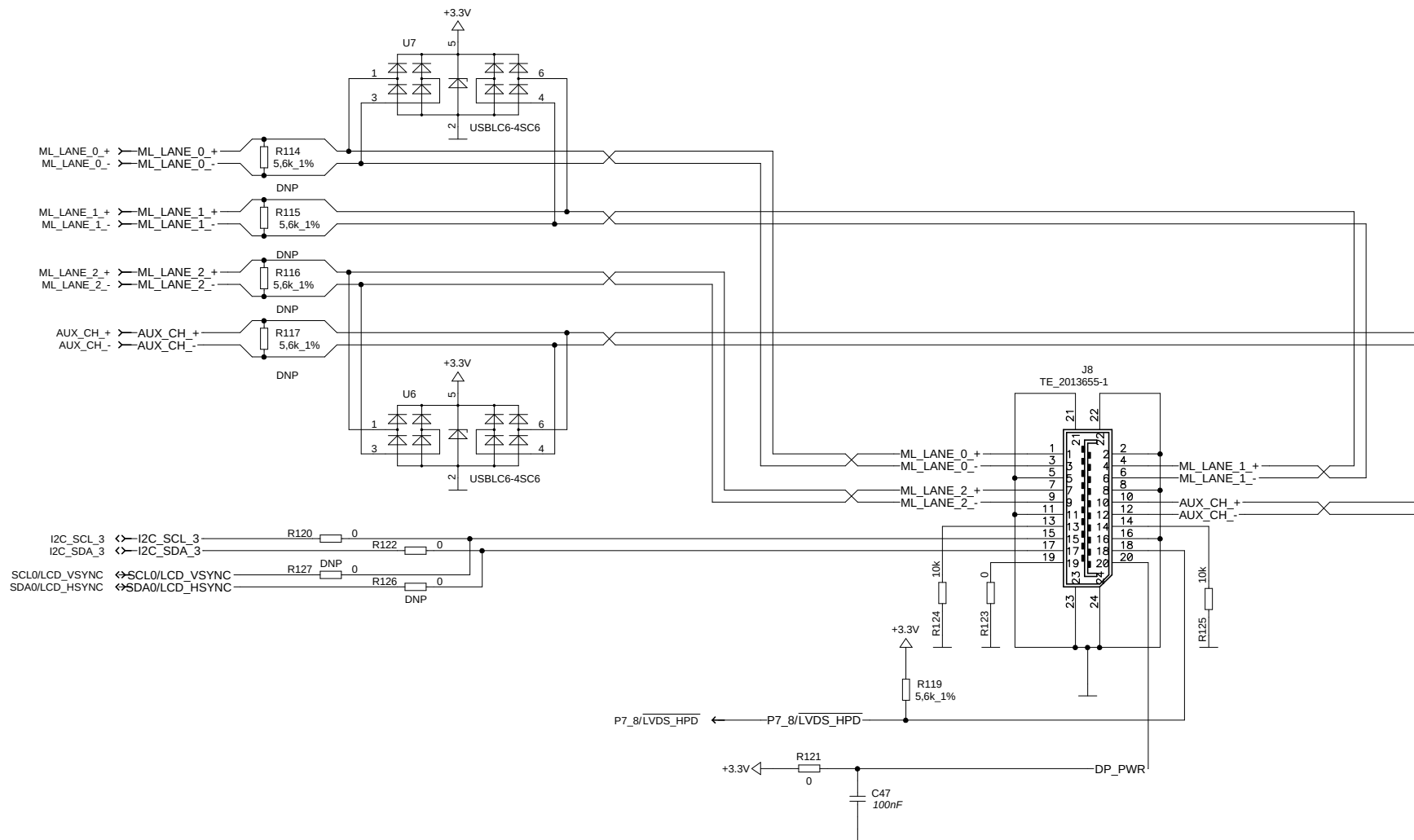
Title		
Jumpers & Pull-Ups		
Size	Number	Rev
A3	mbed VK-RZ/A1H	1.0
Date	27.10.2015	Drawn by
Filename	VK-RZA1H_mbed.sch	D.Todorov
Sheet	3	of
	12	



Title			
MCU Decoupling			
Size	Number		Rev
A3	mbed VK-RZ/A1H		1.0
Date	27.10.2015		Drawn by D.Todorov
Filename	VK-RZA1H_mbed.sch		Sheet 5 of 12



Title		
Memory		
Size	Number	Rev
A3	mbed VK-RZ/A1H	1.0
Date	27.10.2015	Drawn by
Filename	VK-RZA1H_mbed.sch	D.Todorov
Sheet	7	of
	12	



Title			LVDS
Size	Number	Rev	
A3	mbed VK-RZ/A1H	1.0	
Date	27.10.2015	Drawn by	D.Todorov
Filename	VK-RZA1H_mbed.sch	Sheet	10 of 12

1

2

3

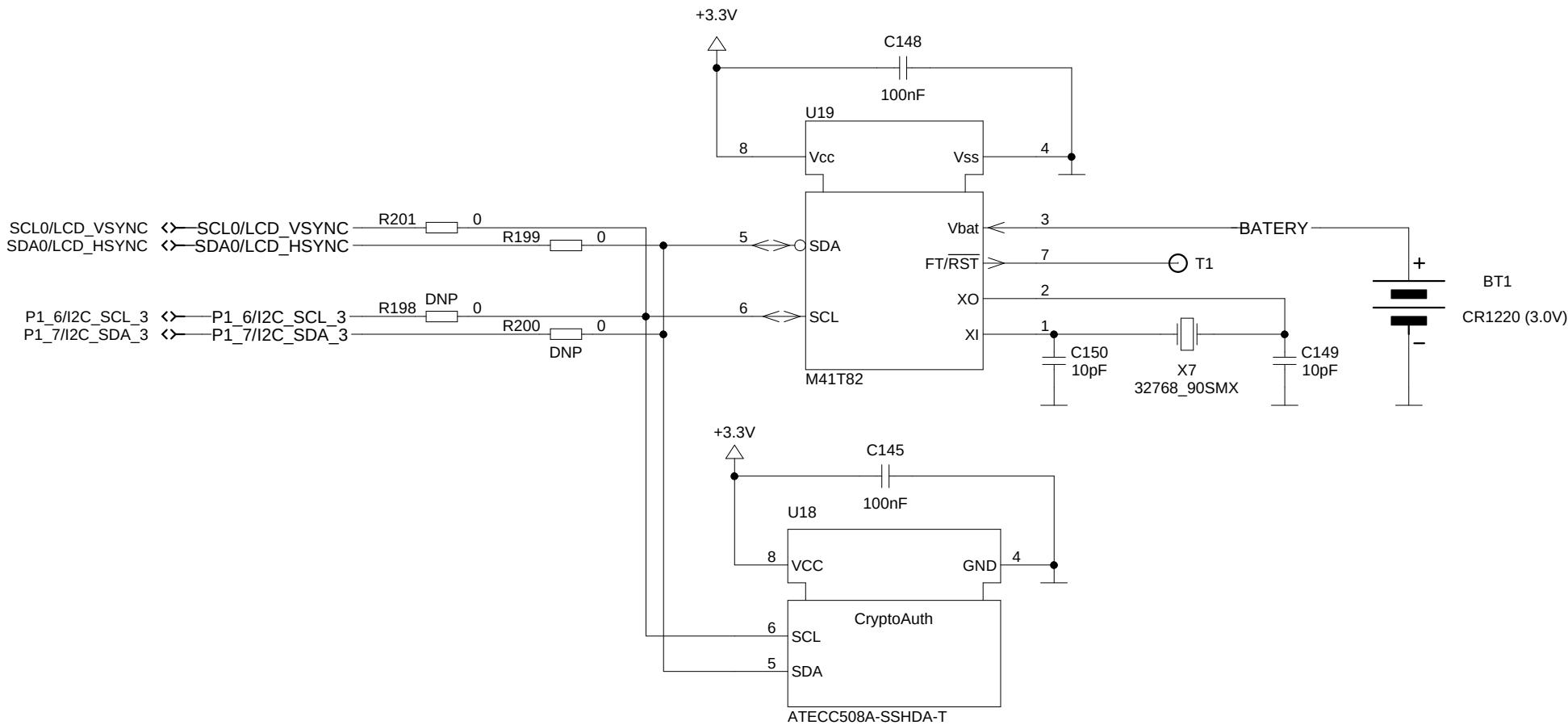
4

1

2

3

4



Title				RTC&Crypto			
Size		Number		Rev			
A4		mbed VK-RZ/A1H		1.0			
Date		27.10.2015		Drawn by		D.Todorov	
Filename		VK-RZA1H_mbed.sch		Sheet		12 of 12	

A

B

C

D

